

NAVI14 GDDR6 4PCS,8L 3xDPs +1xHDMI

105-D332xx-00B RevB Desktop board(110W TGP)

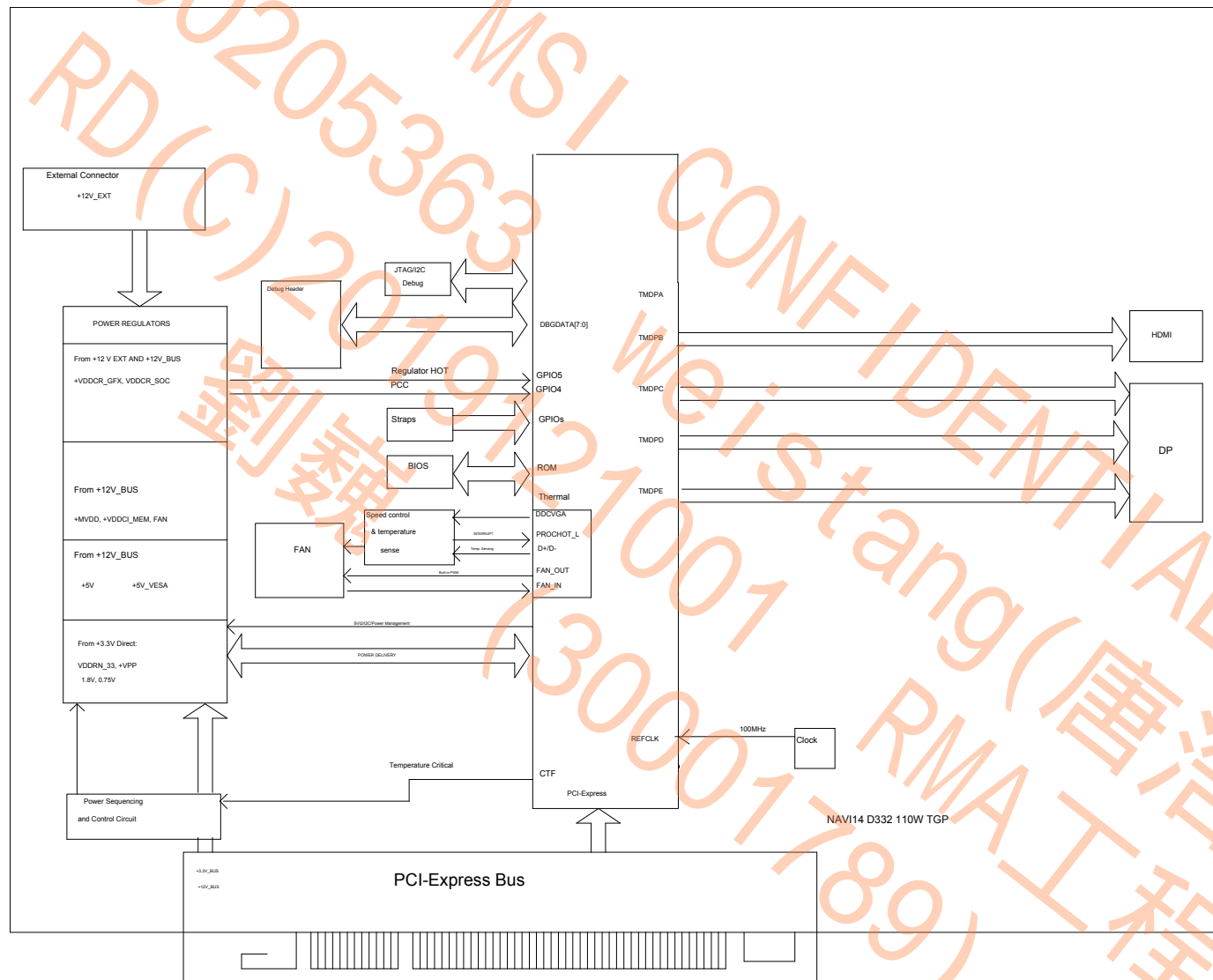
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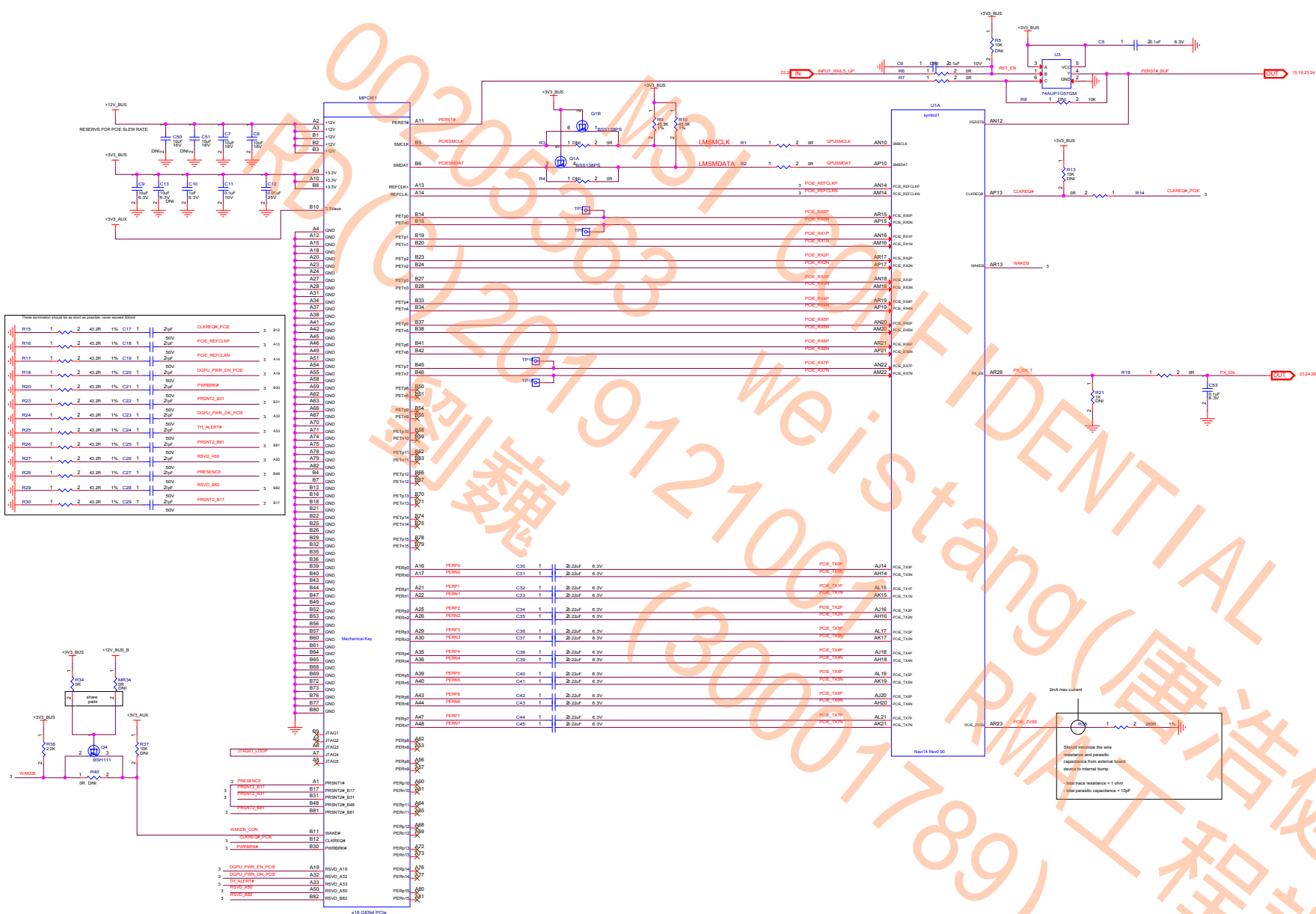
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24	POWER MANAGEMENT		
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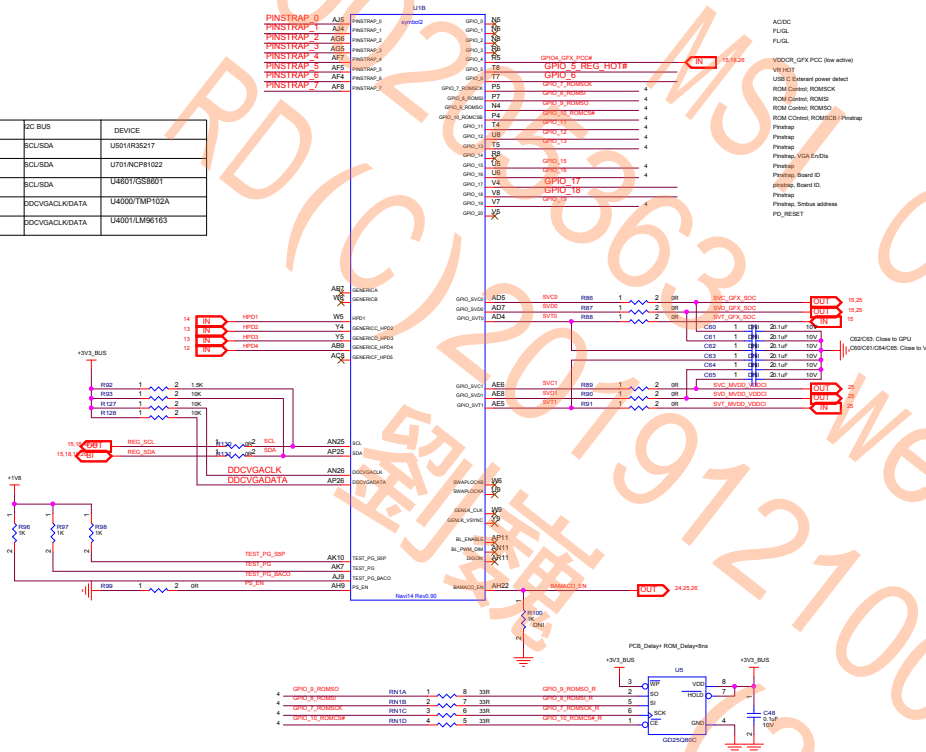
Size Custom	Document Description TOC	Rev 1.0
Date: Monday, September 09, 2019		Sheet 1 of 27



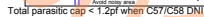


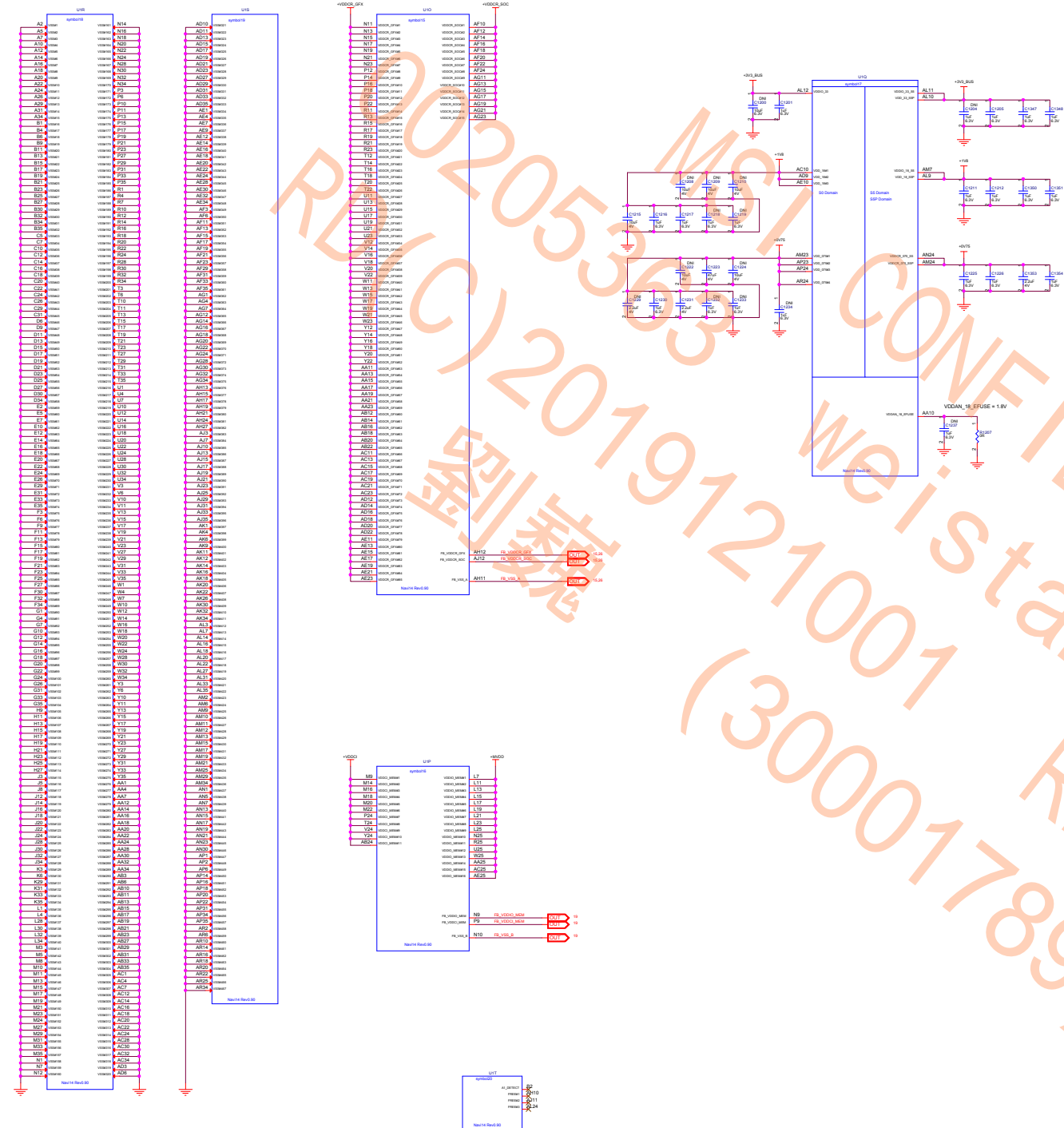
SYMBOL LEGEND	
SW	SWITCH
RES	RESISTOR
ACTIVE	ACTIVE
LOW	LOW
BRNG UP ONLY	BRING UP ONLY
DIGITAL	DIGITAL
GROUND	GROUND
ANALOG	ANALOG
GROUND	GROUND

GPIO	FUNCTION	DC BUS	DEVICE
0x0	VDDOR_GFX/SDC	SCL/SDA	U501/R3S217
0x2	MVSD/VSDC	SCL/SDA	U701/NCP1802
0x3	PC/On-resistor	SCL/SDA	U4801/QS8801
0x48	GS Temperature	DDCVGACK/DCVGAQDATA	U4000/TMP102A
0x4C	EXT SENSOR	DDCVGACK/DCVGAQDATA	U4001/LM98183



User	Internal Default Value	Definition
BIF		STRAP_BIF_GEN4_DIS_A 0: PICH GEN4 supported 1: PICH GEN4 not supported
		PINSTRAP_BIF_CLK_PM_EN 0: CLKREQ power management capability is disabled 1: CLKREQ power management capability is enabled
		PINSTRAP_BIF_LC_TX_SWING 0: Full swing mode 1: Reduced swing mode(half swing)
		PINSTRAP_BIF_VGA_DIS 0: VGA controller capacity enabled 1: The device won't be recognized as the system's VGA controller
DCE		PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: All endpoints connected 1: 8 endpoints connected 2: 5 endpoints connected 3: 4 endpoints connected Default(PINSTRAP3/PINSTRAP4/PINSTRAP5) = 000
		PINSTRAP_AUD[1:0] 1: Audits for DisplayPort only 2: Audits for DisplayPort and HDMI if dongle is detected 3: Audits for both DisplayPort and HDMI Default(PINSTRAP12/GPIO11) = 11
Platform		PINSTRAP_FIG[1:0] - No definition on NV
		PINSTRAP_MVDD_FB_DIVIDER_CONFIG 0: Divider does not exist 1: Divider exists
SMU		PINSTRAP_BFI_MEM_AP_SIZE[2:0] Or PINSTRAP_ROM_CONFIG[2:0] 100: 512KBIT (BT1) M20P05A 101: 1MBIT (BT1) M20P10A 102: 32MBIT (BT1) M20P10A 103: 48MBIT (BT1) M20P10A 104: 32MBIT (BT1) M20P10A 105: 512KBIT (CHN) M20P10A 106: 1MBIT (CHN) M20P10A Default(PINSTRAP2/PINSTRAP3/PINSTRAP4) = 101
		PINSTRAP_SMBUS_ADDR 0: 0x41h 1: 0x40h
SMU		PINSTRAP_BIOS_ROM_EN 0: Disable the external BIOS ROM device 1: Enable the external BIOS ROM device





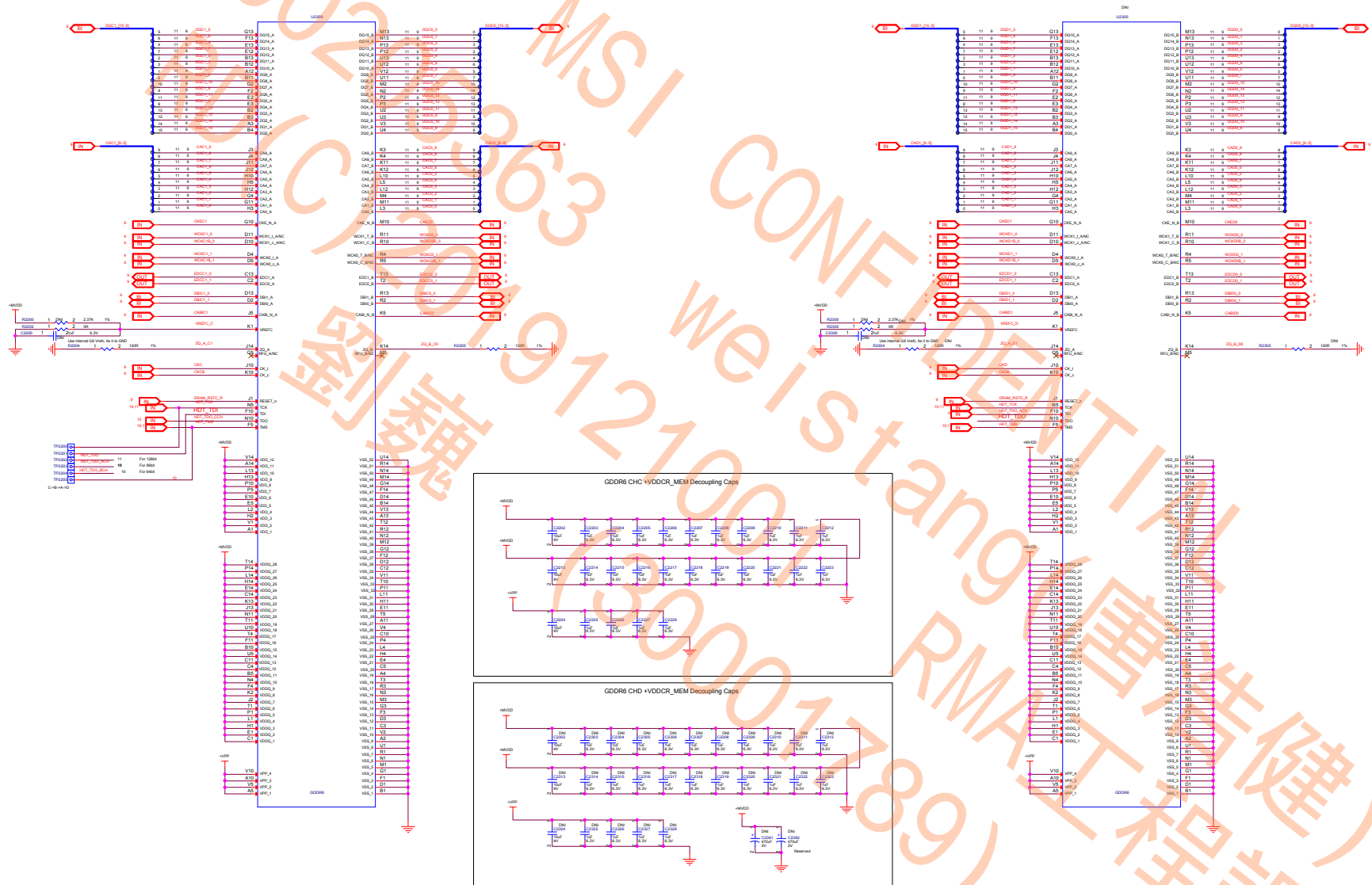




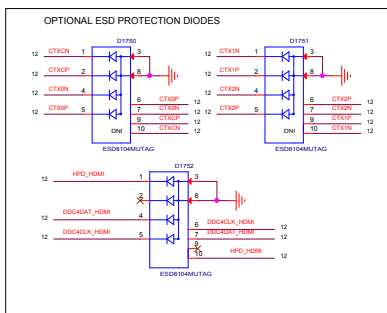
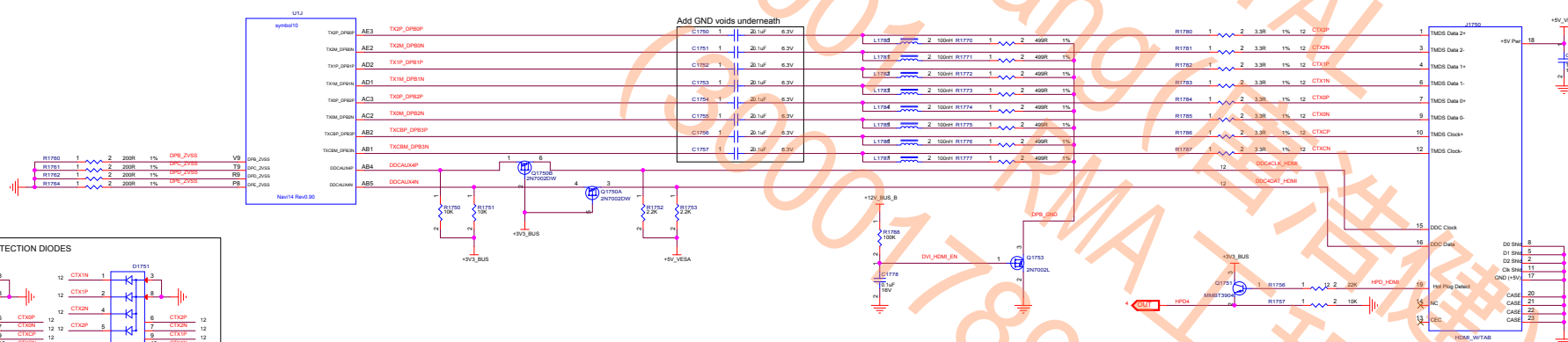
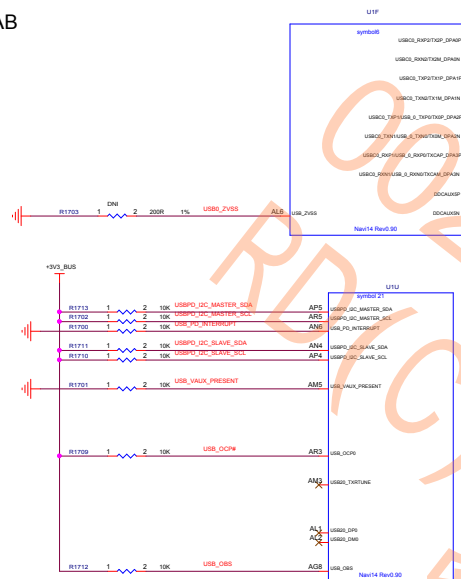


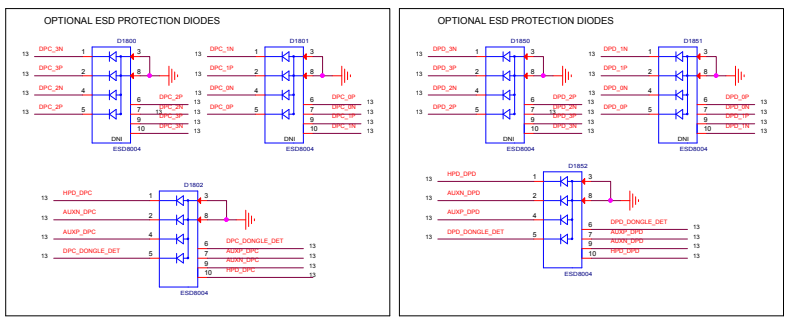


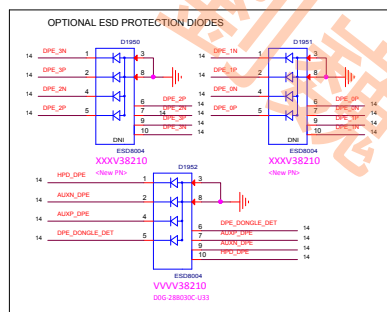
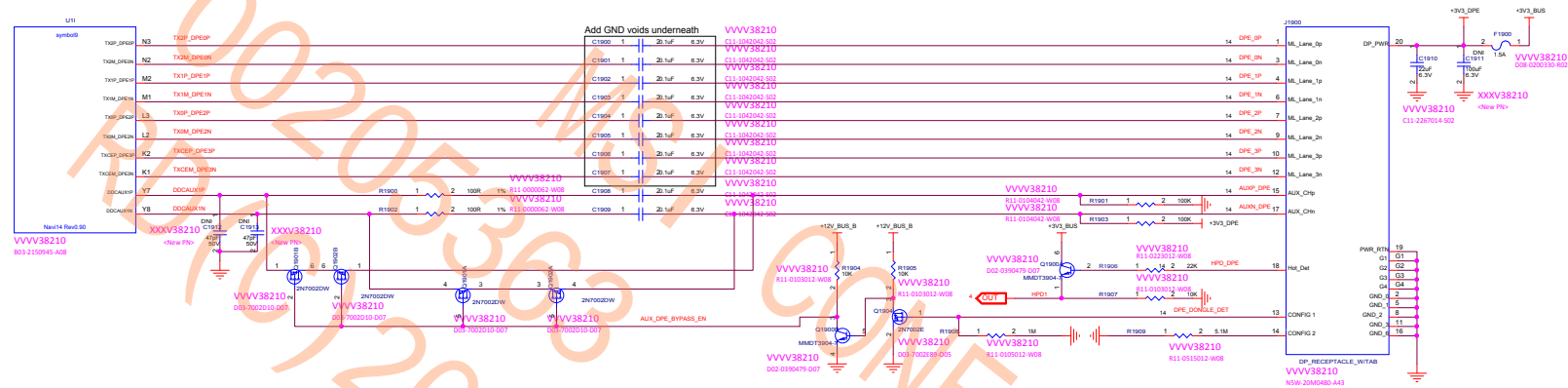




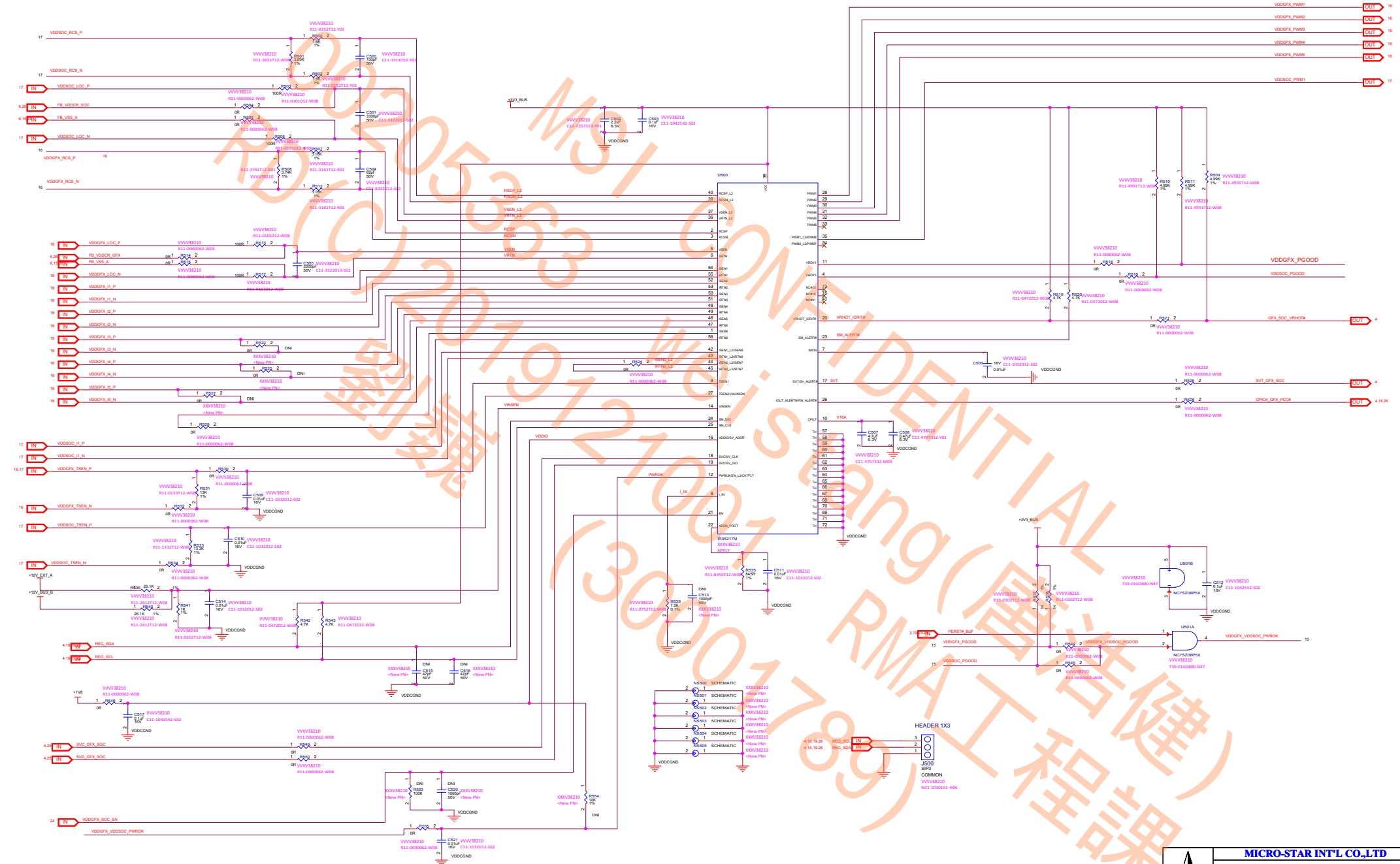
(12) TMDP AB

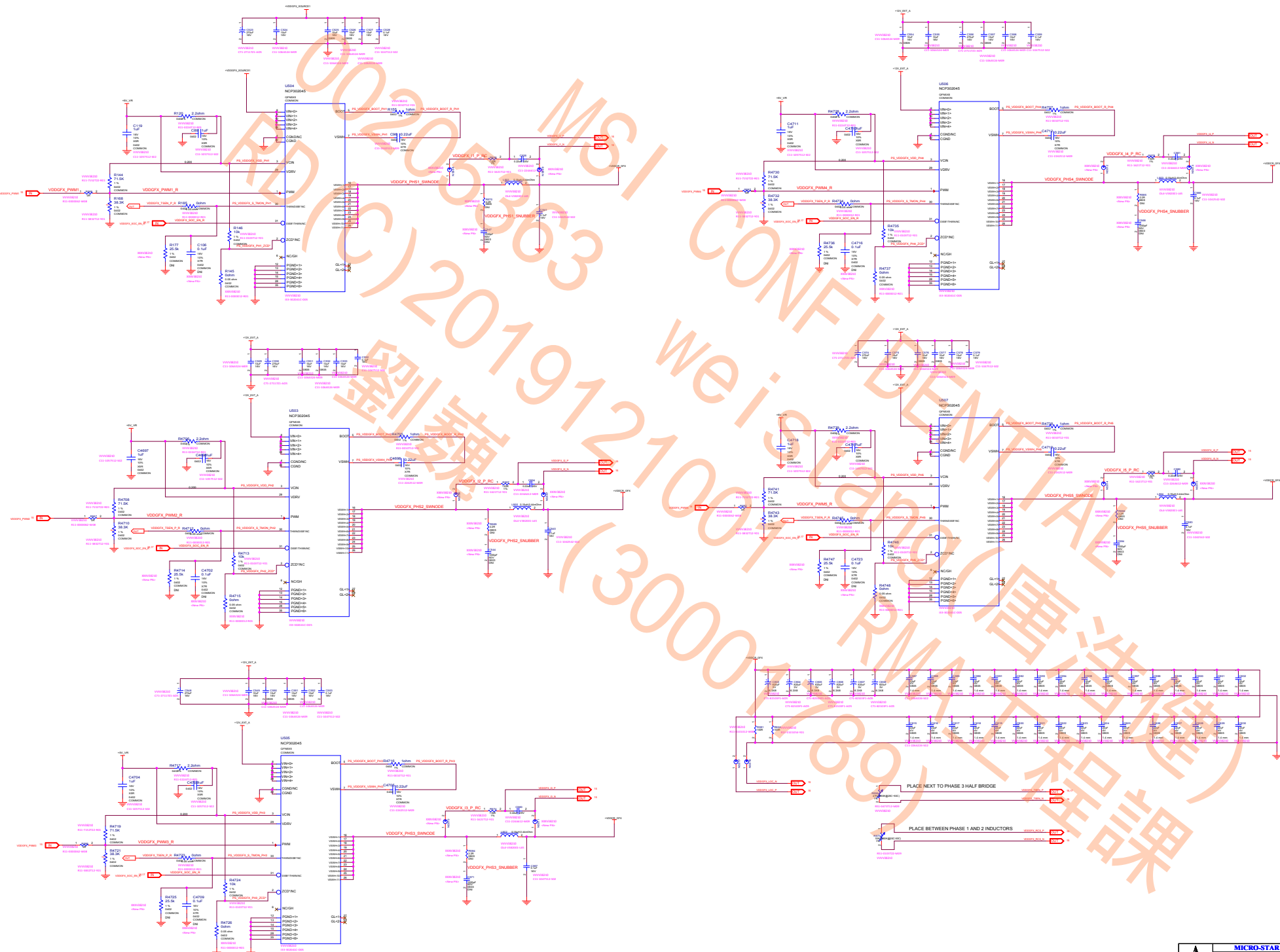




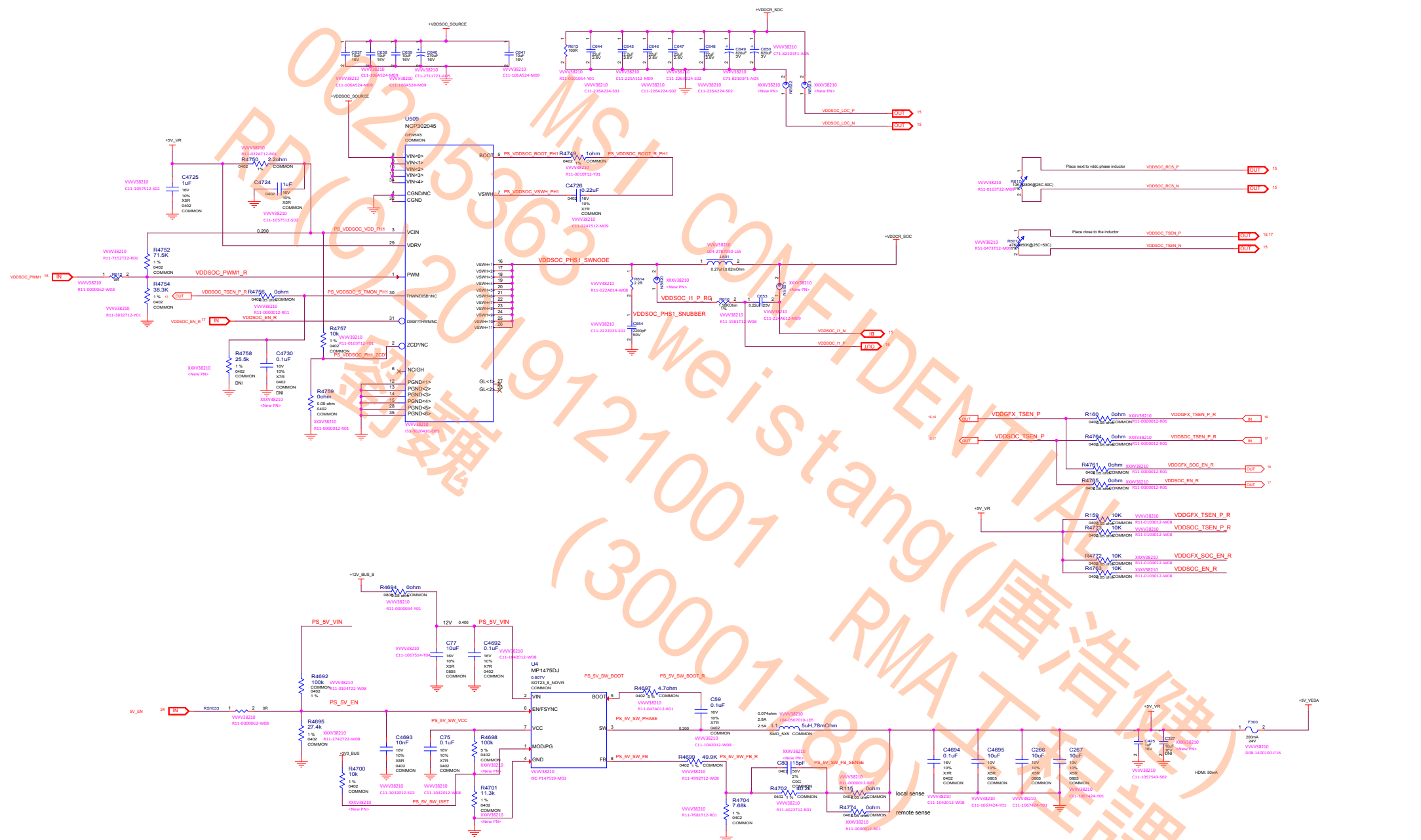


## REG - VDDGFX/VDDSOC CTRL

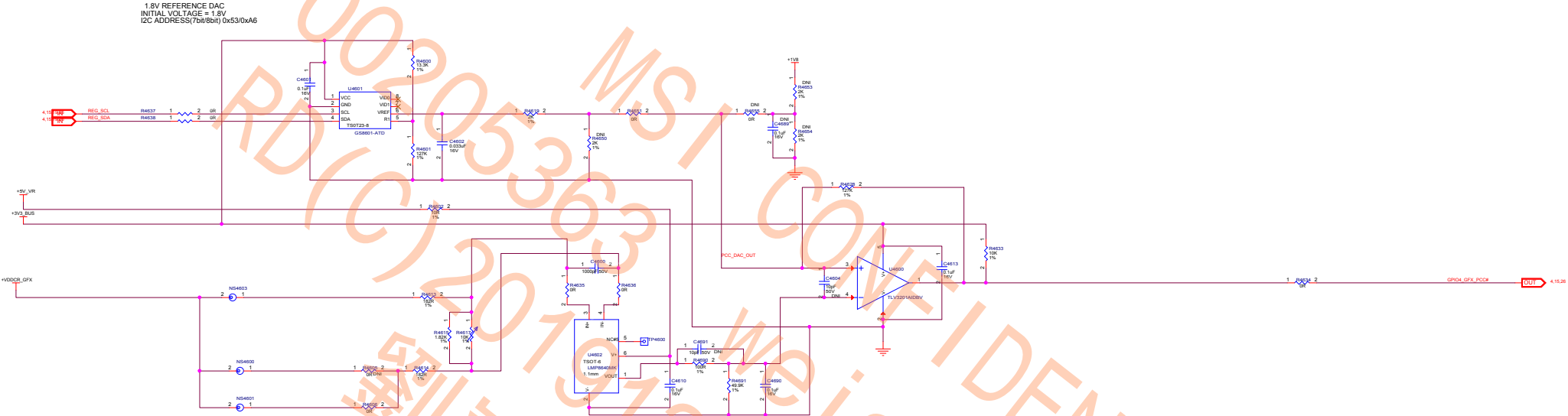


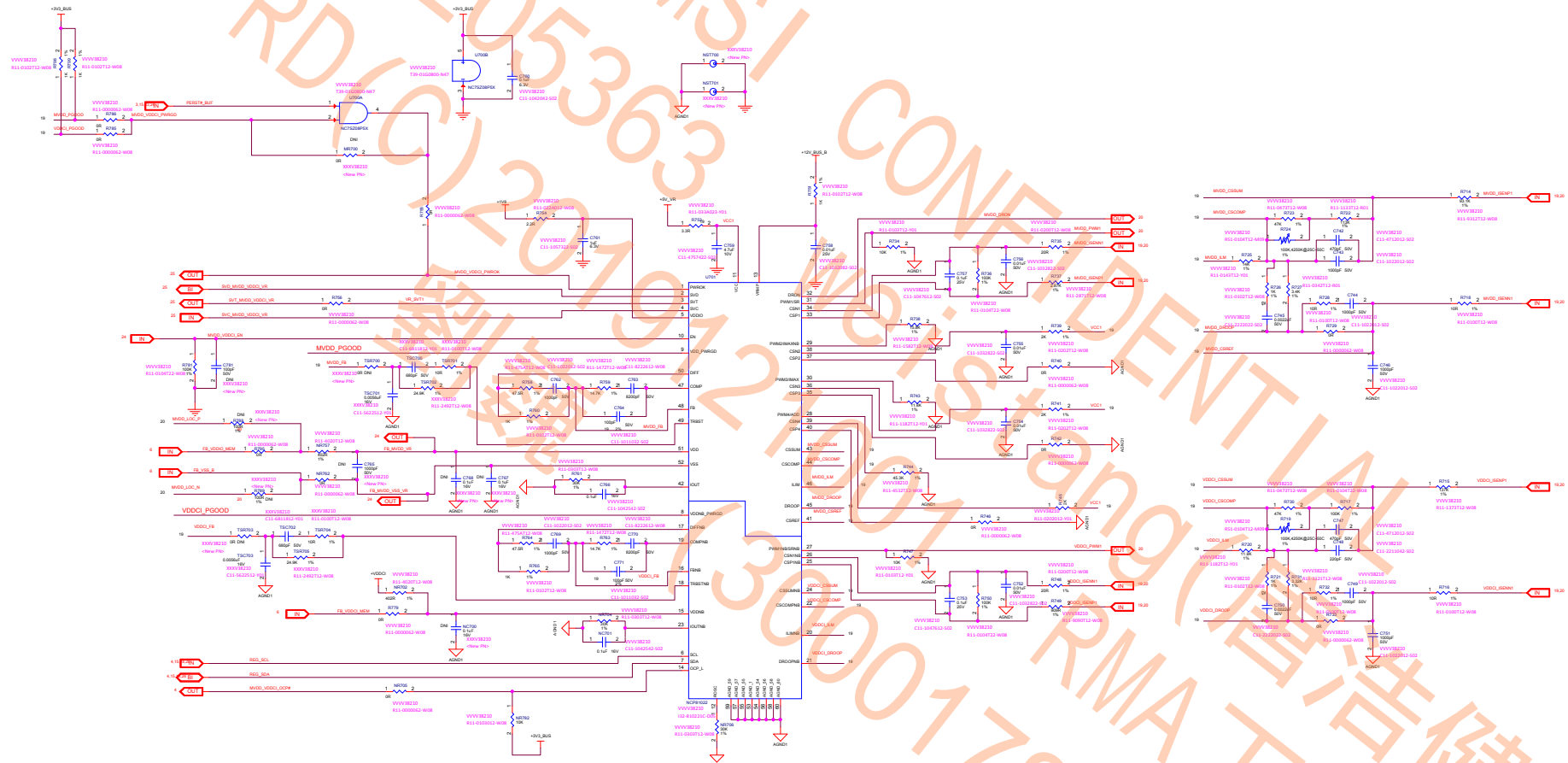


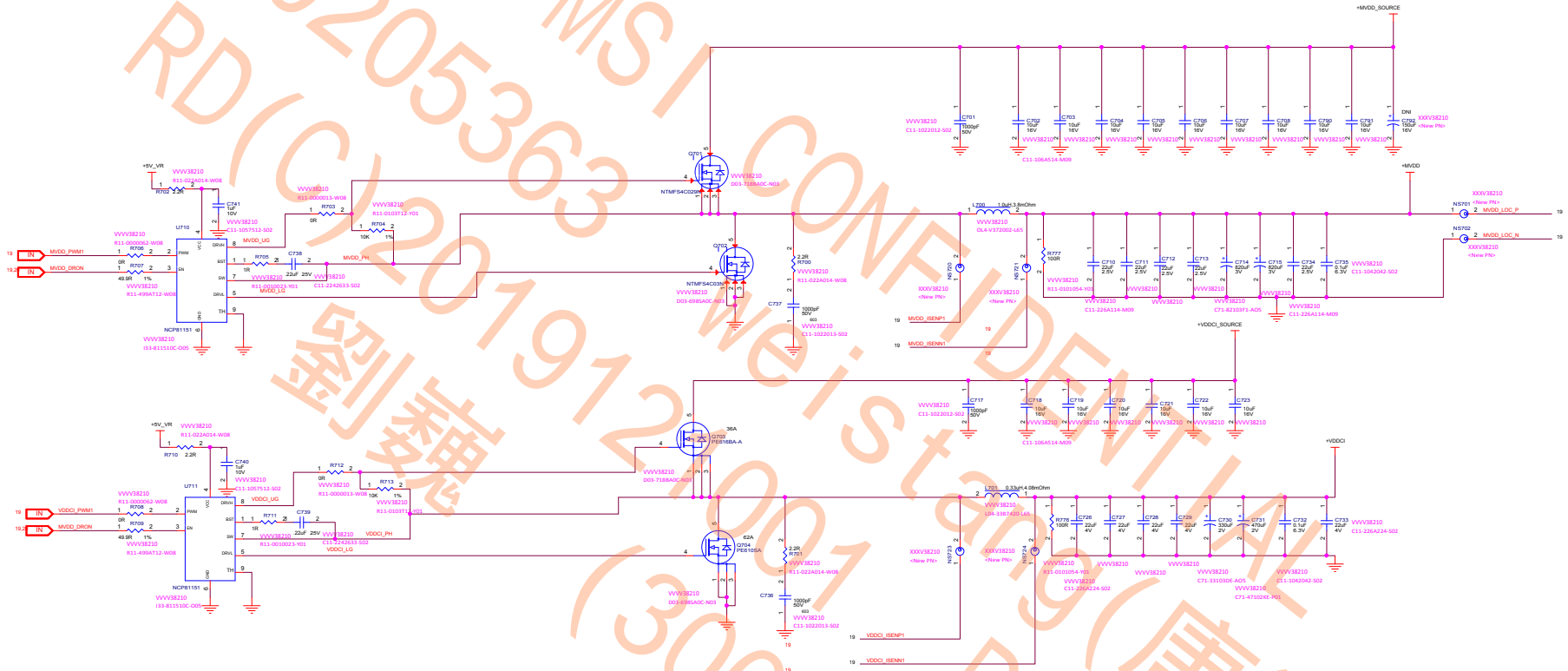


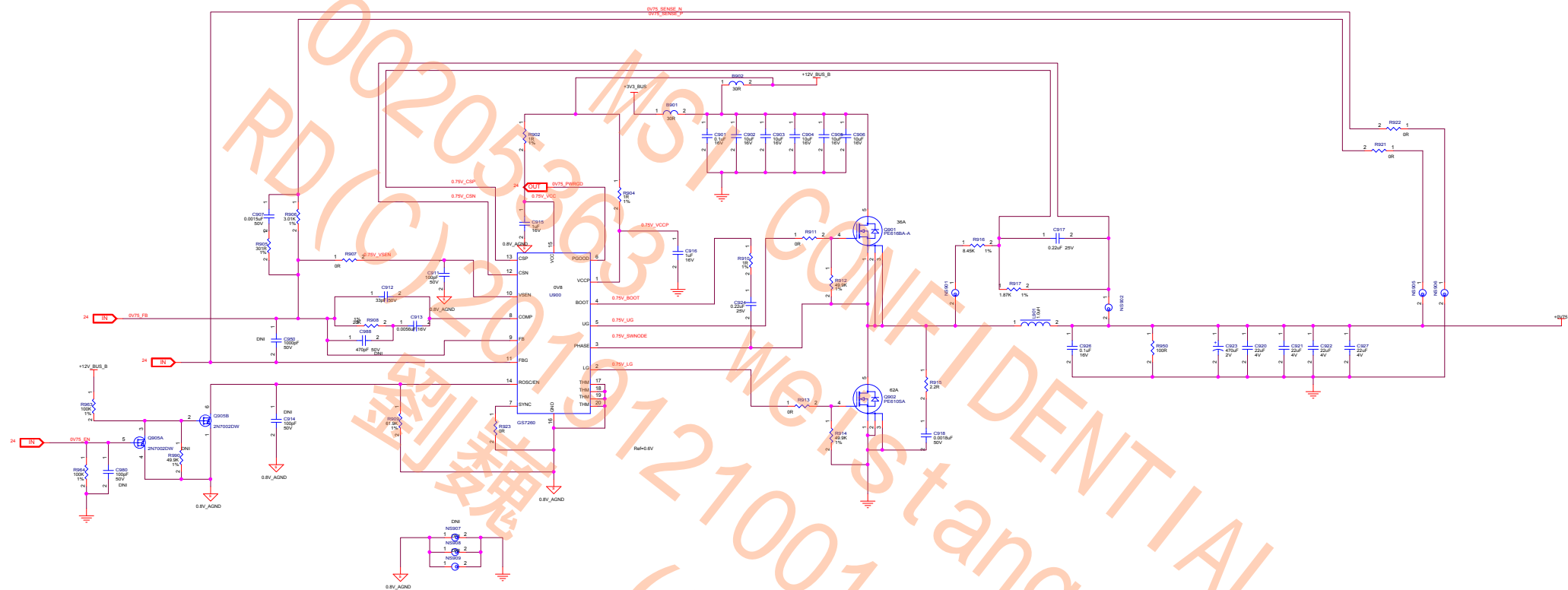


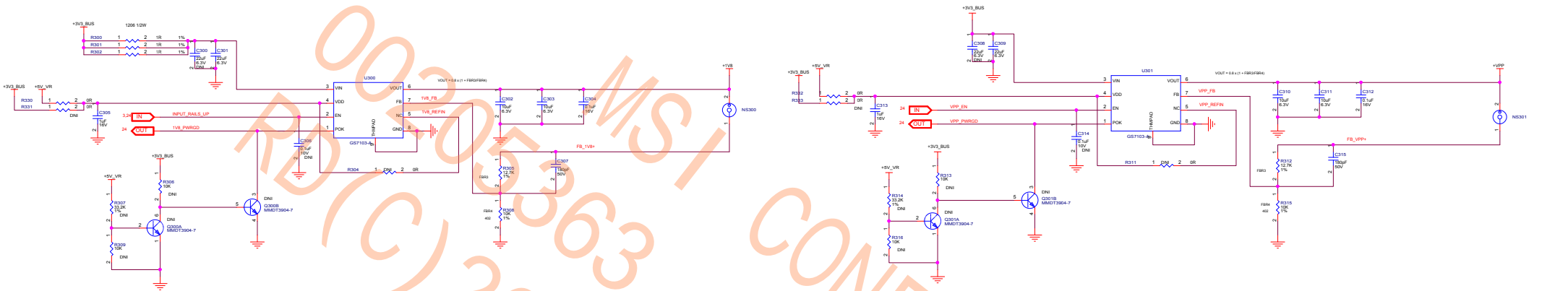
$$0.8V \cdot (1 + 40.2K/7.68K) = 4.9875V$$

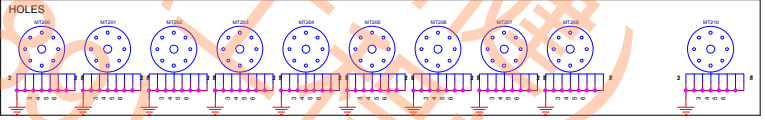
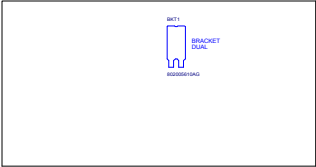
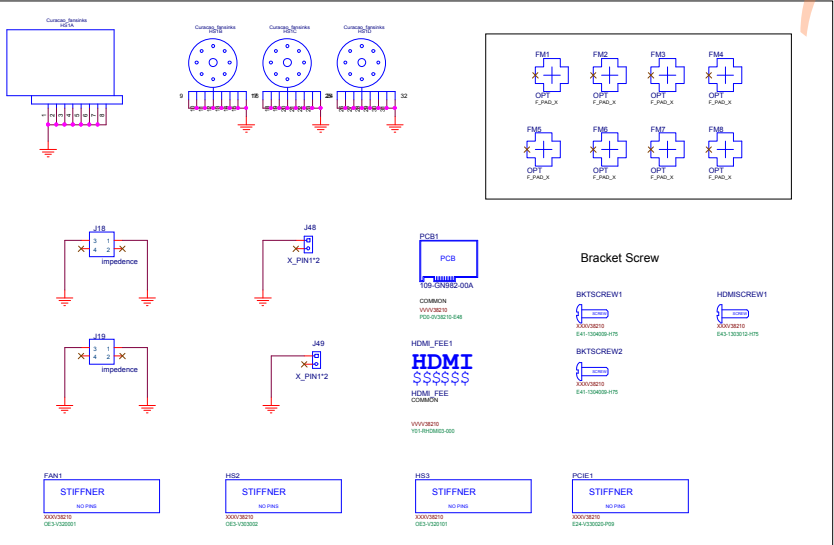
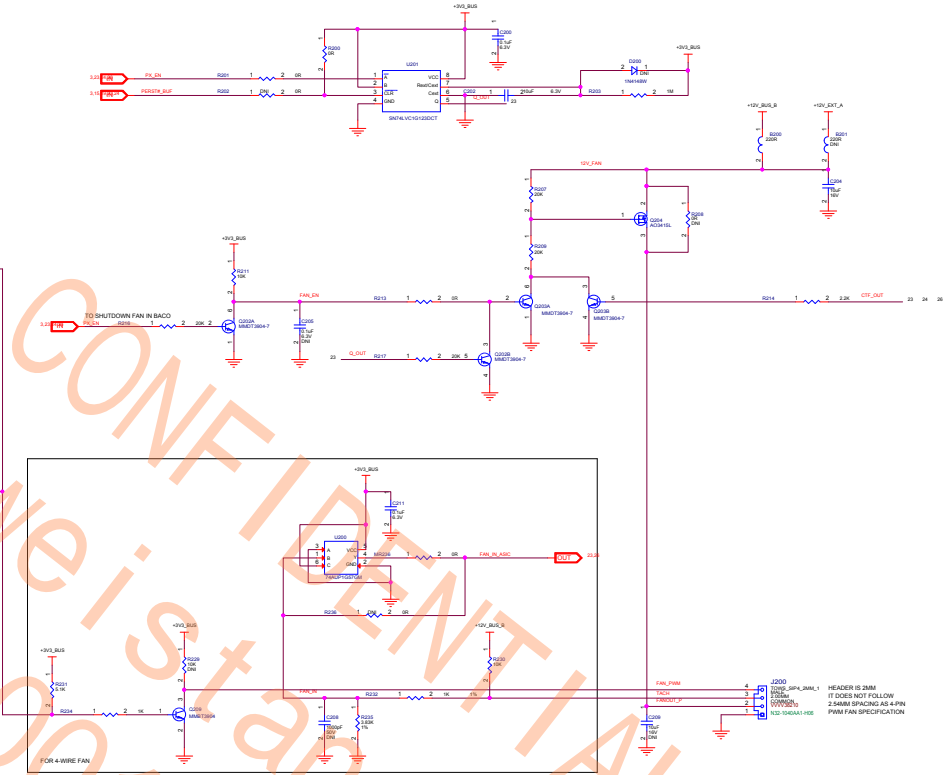
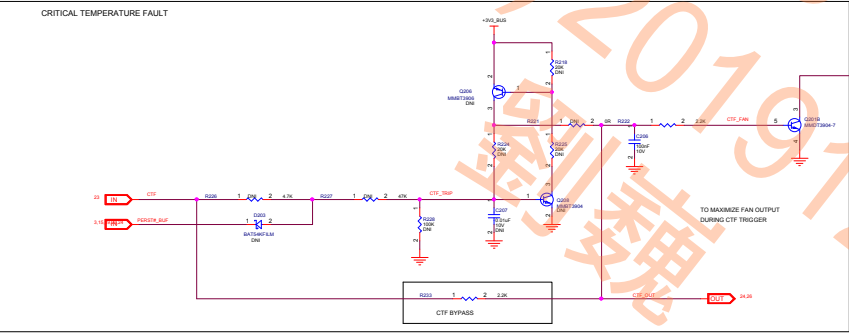
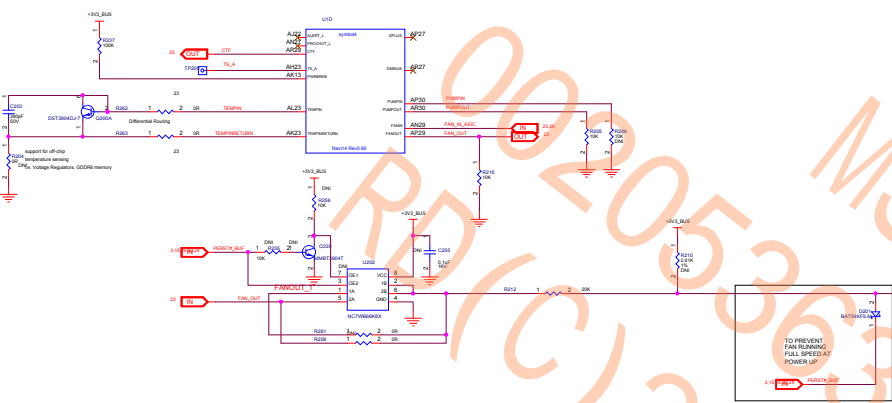


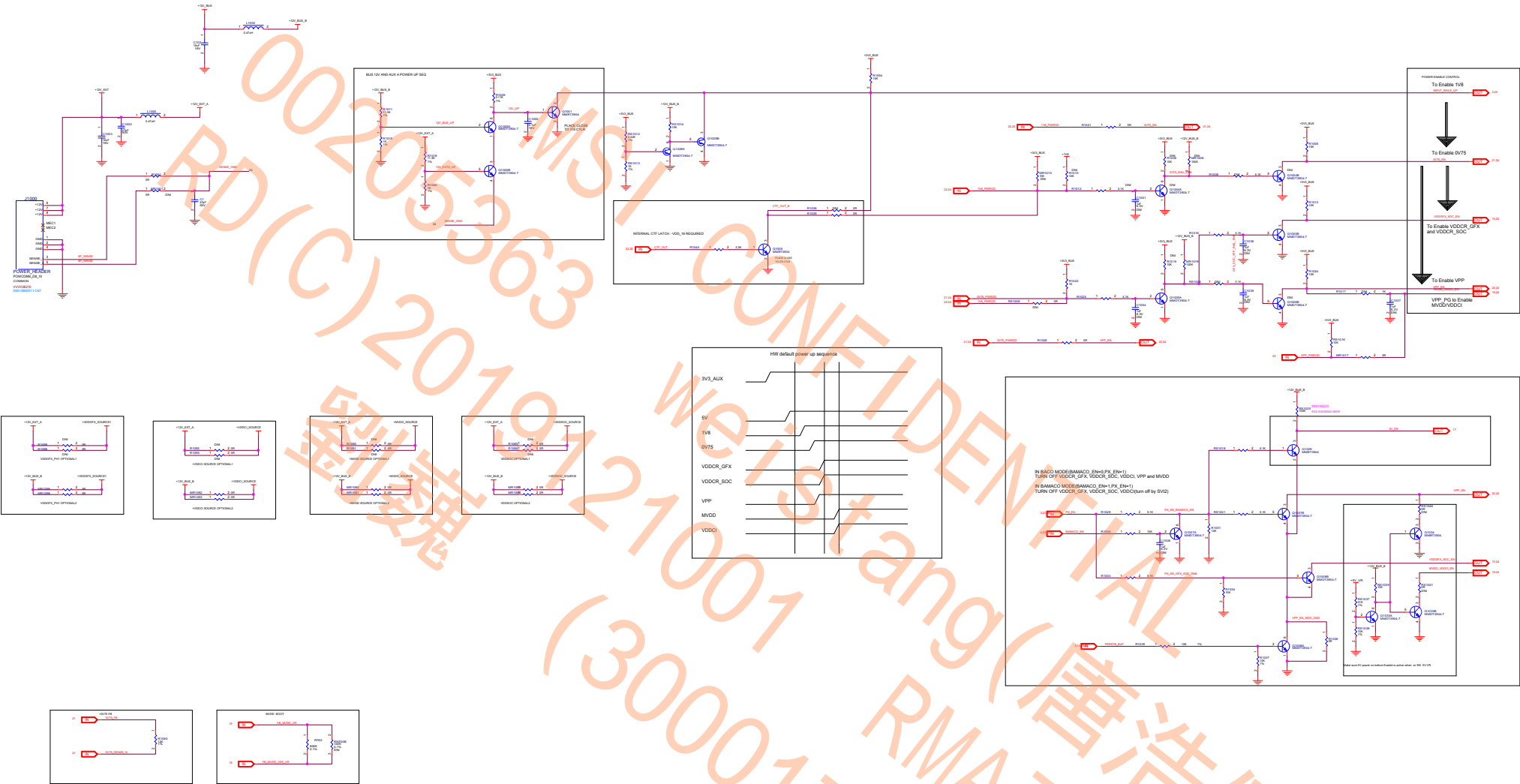




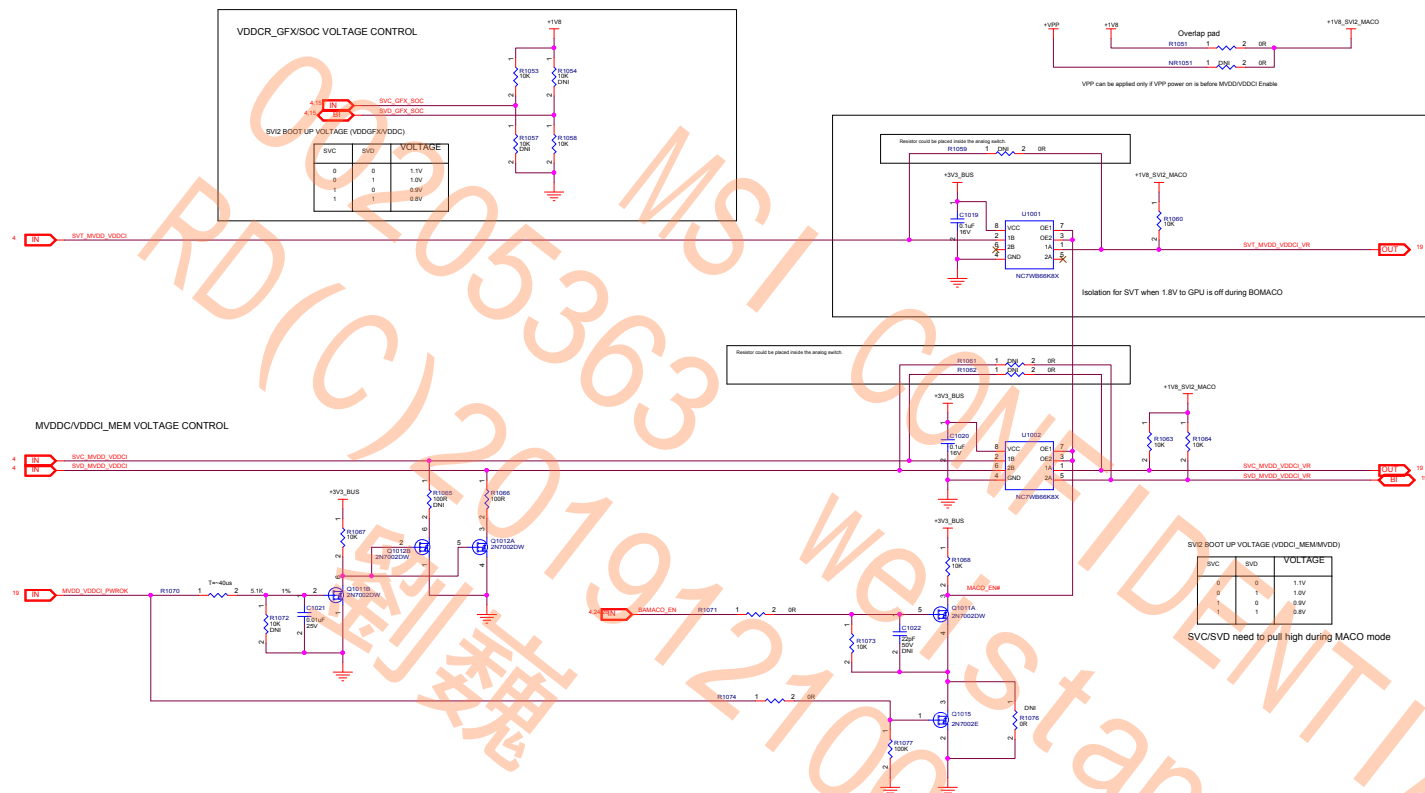




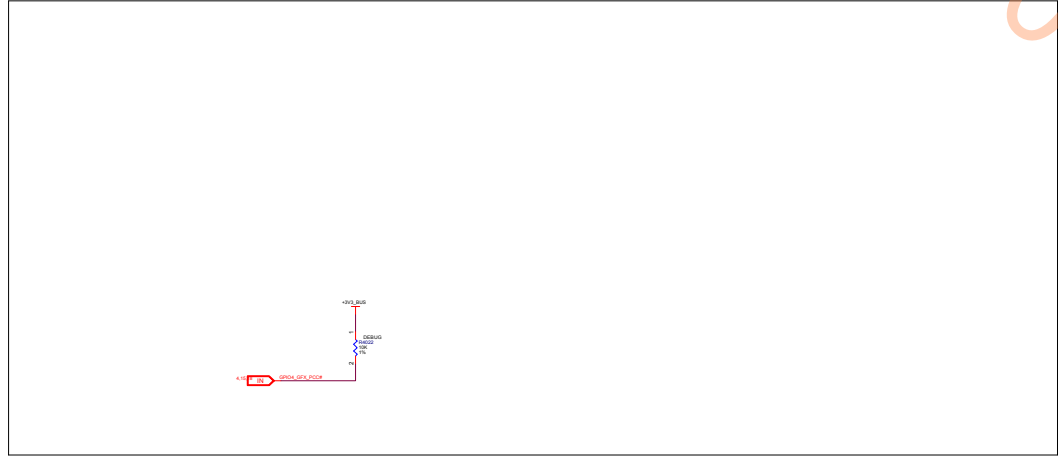
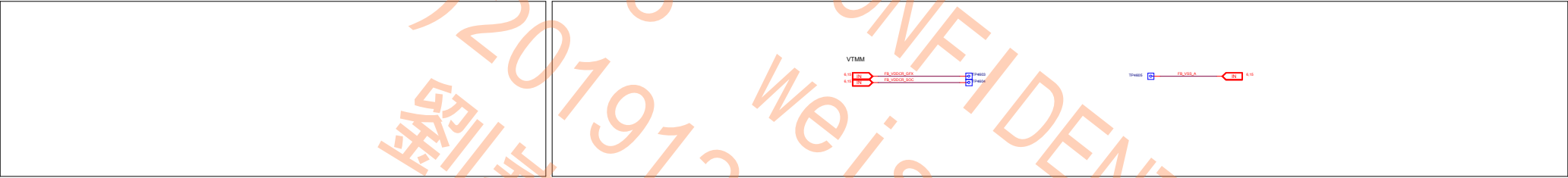
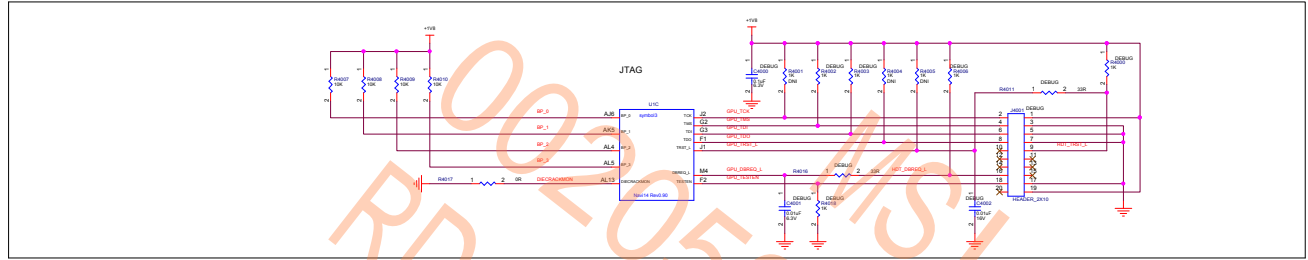








(29) DEBUG CIRCUIT



8

7

6

5

4

3

2

1

AMD



TITLE:

NAV114 XT GDDR6 x16 DT BOARD

DOCUMENT NUMBER:

105-D33200-00B

DATE:

Mon Apr 22 08:33:14 2019

SHEET NUMBER:

27 OF 27

REV:

B

REVISION HISTORY

ENGINEER:

Billy Deng

NOTES:

NOTE

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AMD-PLATFORM HARDWARE ENG  
No.609,HUANKE ROAD  
SHANGHAI,CHINA 201203

SCH Rev

PCB Rev

Date

REVISION DESCRIPTION

1.00

00A

08/09/2018

Initial schematic

1.00

00B

12/26/2018

change all 4172010501G parts to 4172010500G

1.00

00B

04/16/2019

ADD D1752 D1762 D1763 D1765  
ADD R1705 AND CHANGE R1705 LOCAL SENSE POINT  
ADD R1762 R1763 MR1702 MR1703 and reassign gfa phase1-3 input source  
  
ADD R4653 R4654 R4655 C4650  
  
Change T01: 0.53uH520118000G RT49: 909R316050000G NR1704 30K316100200G RT43: 18K2160180200G CT47-AT0P/H170047100G CT48-220uF/H17022100G

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Document Description

REVISION HISTORY

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